Semiconductor Memories

Technology, Testing, and Reliability

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Exhibit A

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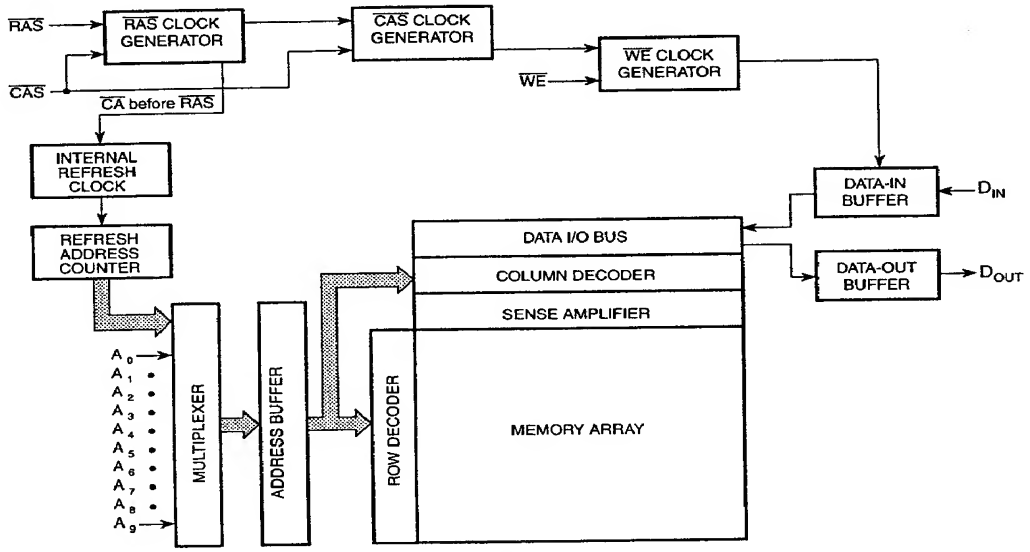
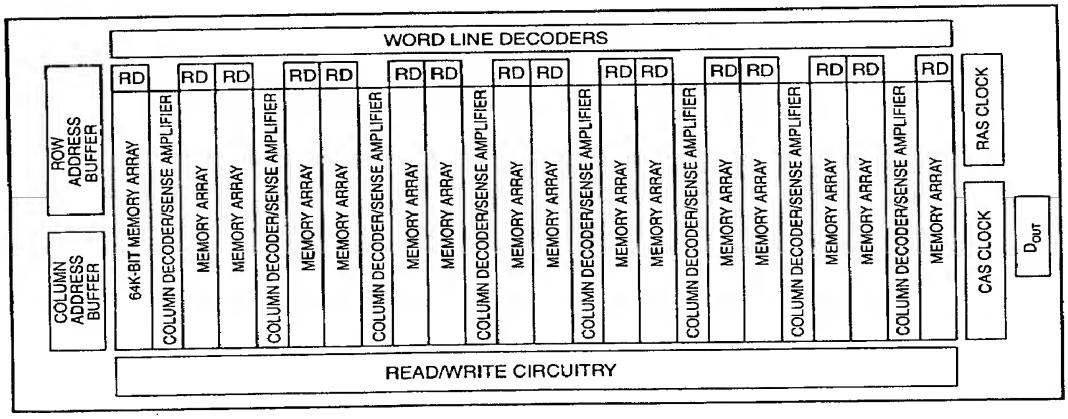
plate reduces the electric field stress across the thinner oxide of the megabit generation storage capacitor and minimizes the influence of supply voltage variations. Some 1 Mb DRAM designs used clock circuitry with address transition detection (ATD) for high-speed operation. There was also improvement in test modes to reduce the memory test time. Several types of parallel test modes were developed which allowed multiple bits (four or eight) to be tested simultaneously instead of one bit at a time.

2.3.2.1 1 Mb DRAM (Example). Figure 2-30(a) shows the block diagram of an NEC 1 Mb DRAM [49] organized as 1,048,576 words × 1 b and designed to operate from a single +5 V supply. This uses advanced polycide technology with trench capacitors which minimizes



(a)



Notes:
[1] The memory is divided into sixteen 64-kbit memory cell arrays.
[2] RD = row decoder/word driver.

(b)

Figure 2-30. (a) Block diagram of 1 Mb DRAM (NEC μPD421000). (b) Chip layout.

TABLE 5-1. The ATS Algorithm Test Sequence. (From [22], with Permission of IEEE.)

State	G_0	G_1	G_2
		WrW_0	WrW_0
	WrW_1		
		RW_0	
		WrW_1	
			RW_0
	RW_1	RW_1	
	WrW_0, RW_0		
			WrW_1, RW_1

1) a sequence generator or test control circuit which is operational only during the test mode, 2) a data-compare circuit on the RAM output data bus, and (3) a means of setting the MDR to all 0s or all 1s word.

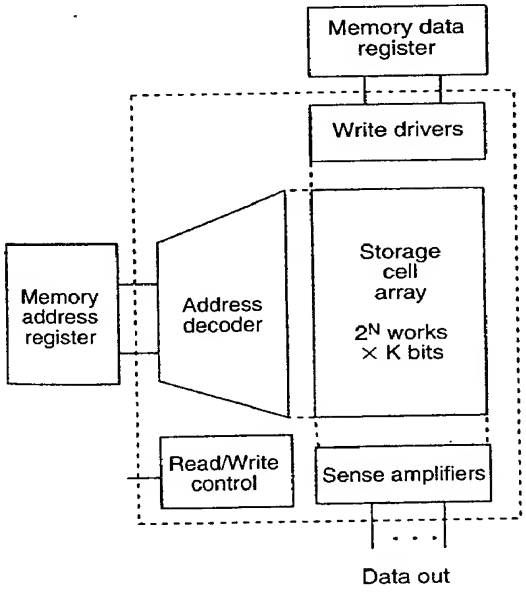


Figure 5-7. A typical RAM structure. (From [22], with permission of IEEE.)

5.2.2 BIST Using 13N March Algorithm

This RAM BIST approach used the 13N March algorithm plus a data-retention test that was discussed in Chapter 4. For a word-oriented SRAM, the words of data instead of the single bits are written to or read from the memory. To detect coupling faults between the cells at the same address, several data words called data backgrounds and their inversions are applied to the SRAM. The register cells are modified to make them scannable so that during the scan test, the SRAM is isolated from its environment. Figure 5-8(a) shows the modified register cell and its logic truth table [23]. A control signal $C1$ controls the register cell and enables the operation mode which is either normal or scan. A second control signal $C2$ enables the self-test mode for data, address, and control generation.

Figure 5-8(b) shows the global architecture for the BIST RAM which requires several logical blocks as follows [23]:

- An address generator (address counter) to generate the test sequence $0 \cdots (N-1)$.
- A wait counter that can be combined with the address counter to count down the wait time for the data-retention test.
- A data generator to produce the data backgrounds and inverted data backgrounds.
- A data receptor that stores or compares the data received from the SRAM during a Read operation.
- A self-test controller to implement the test algorithm, including the control of the RAM and other blocks of self-test logic.

Figure 5-8(c) shows a state diagram of self-test controllers [23].

The self-test begins when all of the flip-flops are initialized and all register cells are in the self-test mode during which the self-controller has full control. Only four states are needed to generate the 13N test algorithm, and the remaining states are used for generating the data-retention test. The conditional jumps